IN THE CLAIMS:

Please cancel Claims 29, 31, 33 to 38, 40, 42 and 44 to 49 and amend the claims as shown below. The claims, as pending in the subject application, read as follows:

1. to 27. (Canceled).

28. (Currently Amended) An information processing apparatus comprising:

processing means; and

mode setting means for setting a mode of a memory,

wherein said processing means sets said mode setting means to an enabled state in which said mode setting means is allowed to set the memory to a power saving mode, and reads issues an instruction fetch transfer for a power saving mode transfer instruction ~~from~~ stored in the memory for setting said processing means to a power saving mode, and

~~wherein said mode setting means sets the memory to the power saving mode while the mode setting means is in the enabled state, and wherein the memory is set to the power saving mode in accordance with information which relates to the setting of said processing means to the power saving mode~~

wherein said information processing apparatus further comprises detecting means for detecting the instruction fetch transfer for the power saving mode transfer instruction and outputting information in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and wherein said mode setting

means sets the memory to the power saving mode in accordance with the information inputted from said detecting means while said mode setting means is in the enabled state.

29. (Canceled)

30. (Previously Presented) An information processing apparatus according to claim 28, wherein if said processing means detects an interruption for returning to the normal operation mode from the power saving mode, said processing means returns a normal operation mode from the power saving mode and invalidates the information relating to the setting of said processing means to the power saving mode, and

wherein said mode setting mode sets the memory in a normal operation mode in accordance with invalidation of the information relating to the setting of said processing means to the power saving mode.

31. (Canceled)

32. (Previously Presented) An information processing apparatus according to claim 28, wherein said mode setting means sets the memory to the power saving mode after an end of memory transfer in progress.

33. to 38. (Canceled)

39. (Currently Amended) A power saving controlling method for a processor and a memory, the method comprising:

an enabled state setting step of setting a memory controller for controlling the memory to an enabled state in which the memory controller is allowed to set the memory to a power saving mode;

~~a reading~~ an issuing step ~~of reading~~ issuing an instruction fetch transfer for a power saving mode transfer instruction ~~from~~ stored in the memory for setting the processor to a power saving mode; ~~and~~

a detecting step of detecting the instruction fetch transfer for the power saving mode transfer instruction; and

an outputting step of outputting information in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and

a power saving mode setting step of setting the memory to a power saving mode while the memory controller is in the enabled state[[,]] ~~and wherein the memory is set to the power saving mode~~ in accordance with ~~information which relates to the setting of the processor to the power saving mode~~ the information outputted in said detecting step while the memory controller is in the enabled state.

40. (Canceled)

41. (Previously Presented) A power saving controlling method according to claim 39, further comprising:

a returning step of returning the processor to a normal operation mode from the power saving mode in accordance with an interruption;

an invalidating step of invalidating the information relating to the setting of the processor in the power saving mode in accordance with the returning to the normal operation mode of the processor; and

a returning step of returning the memory to a normal operation mode in accordance with invalidation of the information relating to the setting of the processor to the power saving mode.

42. (Canceled)

43. (Previously Presented) A power saving controlling method according to claim 39, wherein the memory is set to the power saving mode at said power saving mode setting step after an end of memory transfer in progress.

44. to 49. (Canceled)

50. (Previously Presented) An information processing apparatus comprising:

processing means;

setting means for setting a mode of a memory; and

detecting means for detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting said processing means to a power saving mode, wherein said signal is detected on a bus to which said processing means is connected, and

wherein said setting means sets the memory to the power saving mode in a case where said setting means is allowed to set the memory to the power saving mode and where said signal is detected by said detecting means.

51. (Previously Presented) An information processing apparatus according to claim 50, wherein the signal detected by said detecting means relates to an instruction fetch transfer for fetching the power saving mode transfer instruction from the memory for setting said processing means to the power saving mode.

52. (Previously Presented) An information processing apparatus according to claim 50, wherein said setting means sets the memory to the power saving mode after an end of memory transfer in progress in a case where said setting means is allowed to set the memory to the power saving mode and where the signal relating to reading the power saving mode transfer instruction from the memory for setting said processing means to the power saving mode is detected by said detecting means.

53. (Previously Presented) A power saving controlling method for a processor and a memory, the method comprising:

a detecting step of detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode , wherein said signal is detected on a bus to which the processor is connected;

an allowing step of allowing a memory controller to set the memory to a power saving mode; and

a setting step of setting the memory to the power saving mode in a case where the memory controller is allowed in said allowing step to set the memory to the power saving mode and where said signal is detected in said detecting step.

54. (Previously Presented) A power saving controlling method according to claim 53, wherein the signal detected in said detecting step relates to an instruction fetch transfer for fetching the power saving mode transfer instruction from the memory for setting the processor to the power saving mode.

55. (Previously Presented) A power saving controlling method according to claim 53, wherein the memory is set in said setting step to the power saving mode saving mode after an end of memory transfer in progress in a case where the memory controller is allowed in said allowing step to set the memory to the power saving mode and where the signal relating to reading the power saving mode transfer instruction from the memory for setting the processor to the power saving mode is detected in said detecting step.